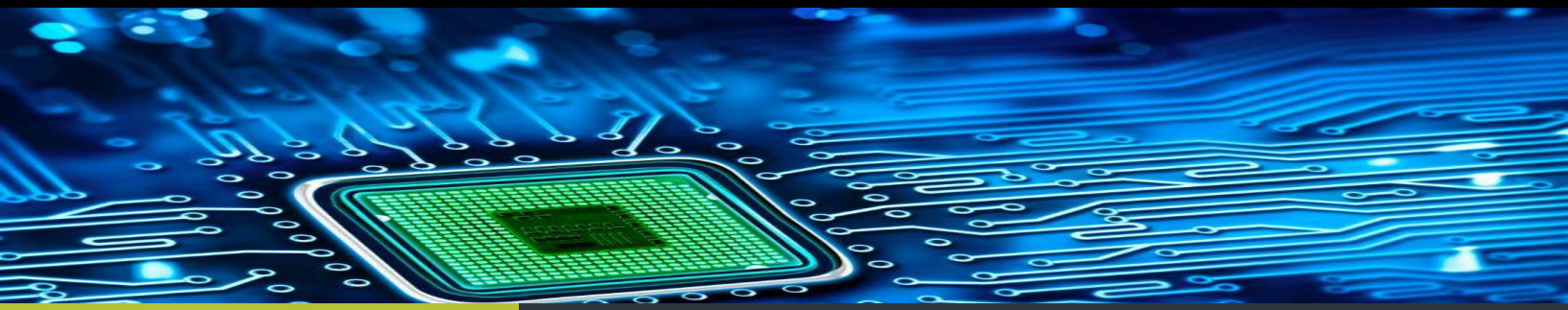
AICTE sponsored National Seminar
on
"Design Issues in Low Power VLSI Domain"
November 08, 2017

Organized by Department of Electronics and Communication Engineering
Guru Nanak Dev Engineering College, Ludhiana

Supported by: All India Council for Technical Education (AICTE), New Delhi



Topics of Focus

Papers are invited in the following topics (but not limited to):

- **CMOS analog , mixed signal and digital circuits**
- **Need of low power design and its impact on system design**
- **Power analysis and Optimization techniques for low power and ultra-low power circuits**
- **Deep-submicron and nanometer devices and circuits**
- **Memory circuits and systems**
- **Device physics design and circuits using non-silicon materials**
- **Design automation using CAD tools**
- **Design for manufacturability, testability and BIST**
- **SoC and NoC architectures**
- **System in package design**

Address for Correspondence
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About the Seminar

The objective of the seminar is to bring professional engineers, academicians and research scholars of matching interests on a common platform to share innovative ideas, experiences and knowledge in various fields of VLSI Design, Test and Technology. The scientific program will consist of paper presentation in technical sessions. In addition, keynote lectures, presentation by industry professionals will be conducted during the event. Such interactions will facilitate better understanding about technological developments all across the globe amongst the peers. This seminar will certainly ignite the minds of researchers for understanding more interdisciplinary collaborative research for upgradation of technology.

Important Dates

Paper Submission	**Nov.03, 2017**
Paper Acceptance	**Nov.06, 2017**
Paper Registration	**Nov.07, 2017**

Registration Fee: Rs 200 /-

The fee can be paid in cash (on the spot) or draft payable in favour of Principal, GNDEC, Ludhiana
One of the authors must register for inclusion of paper in Seminar.

Guidelines for Paper

- Times New Roman MS word, 12 point Font size, Single column, 1.5 Line Spacing, **word limit: 1500-2000 words.**
- The first page of manuscript must have **title of paper, author(s) name, organization affiliation, email address.**
- **Table, illustration, charts, figures etc. should be serially numbered**
- **Reference list should be alphabetically arranged.**
- **Selected papers are to be presented in the seminar.**

Registration Form

AICTE sponsored National seminar on

"Design Issues in Low Power VLSI Domain" (8th November, 2017)

Title of paper		*Registration number:
Name		
Designation		
Department		
College/ Institute		
E-mail ID		
Address		
Mobile no.		
Accommodation required	☐ Yes ☐ No	
Amount of Fee		Mode of payment: Cash ☐ / Draft ☐

Signature of candidate

* Registration number will be allotted after the submission of paper.

NOTE: 1. **Scanned copy of Registration form** and **draft** MUST be submitted to **ece@gndec.ac.in** by November 07, 2017. Hard copy of the application form is to be submitted during registration on November 08, 2017.

2. **The *accommodation*** can be provided in institute ***guest house/hostel*** on **nominal charges** as per request.