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Total No. of Questions : 08]

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Paper ID [EC521]

(Please fill this Paper ID in OMR Sheet)

M.Tech. (Sem. - 1st)

MICROELECTRONICS TECHNOLOGY (EC - 521)

Time : 03 Hours

Maximum Marks : 100

Instruction to Candidates:

- 1) Attempt any Five questions.
- 2) All questions carry equal marks.

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- Q1)** (a) Compare the relative merits of three forms of pull-up for an inverter circuit. What is the best choice for realization in (i) nMOS technology (ii) CMOS technology.
- (b) Explain the working principle and characteristics of enhancement and depletion model transistors.
- Q2)** (a) Derive the required ratio between pull-up to pull-down ratio if an nMOS inverter is to be driven from another nMOS inverter.
- (b) Discuss the MOS transistor circuit model.
- Q3)** (a) Draw the stick diagram and a mask layout for an 8 : 1 nMOS inverter circuit. Both the input & output point should be on the polysilicon layer.
- (b) Discuss Lambda-based design rules with suitable examples.
- Q4)** (a) Discuss double metal, single polysilicon CMOS design rules with examples.
- (b) A particular layer of MOS circuit has a resistivity $\rho = 1$ ohm. cm. A section of this layer is 55 μm long and 5 μm wide and has a thickness of 1 μm . Calculate the resistance from one end of this section to the other.
- Q5)** (a) What are super buffers. Explain.
- (b) Discuss the architectural issues for a VLSI subsystem.

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- Q6) (a) Discuss the various limitations of scaling.
(b) Discuss the various effects of scaling.
- Q7) (a) What are clocked sequential circuits? Explain with examples.
(b) Design a stick diagram for a priority encoder circuit.
- Q8) Write short notes on the following :
(a) Latch-up on CMOS circuits.
(b) Switch logic.

