Report for IEEE Workshop on Advanced Semiconductor Packaging

Venue: **IIT, Ropar**

Date: **7th November, 2015**

Participants from GNDEC, Ludhiana

1. Er.Gagandeep Singh Sodhi

2. Er. Arvind Dhingra

3. Er. Vivek Thapar

4. Er.Navneet Kaur

The workshop started with lecture by Pf. Madhavan Swaminathan, John Pippin Chair Professor, Georgia Institute of Technology, Atlanta, USA via video conferencing. Pf. M. Swaminathan gave a brief outline of role of electronic systems packaging. He then defined the problems faced during packaging such as power delivery, signal integrity, RF connects. He also highlighted the research areas for upcoming researchers. He also advised faculty, students and industry to come together and work together as a team for finding packaging solutions.

In session 2, Dr.Arun Chandrasekhar, Sr. Package designer, Intel Bangalore stressed upon the multidisciplinary aspects of semiconductor packaging. He started from basics of packaging while citing the fact that performance per unit volume has multiplied significantly. He gave an insight on packaging hierarchy. He also brought out the changes taking place in semi conductor packaging. He brought out the primary package functions, its attributes while supporting his thoughts with examples of some popular packaging types. In multi disciplinary nature of packaging, he gave the factors that influence packaging design and also the challenges associated with packaging. His session ended with opportunities available.

In session 3, Dr. Dipanjan Gope, Electrical Communication Engineering, IISc, Bangalore gave his views on Opportunities in 3D full wave solutions for SI and PI applications. He started with the very basic nature of electronic products, system level trends. He then dwelled on the system level challenges. He then talked on package board EM tools. He gave an analogy for packaging using compression with astronomy. He also gave an insight on model to hardware technique using EMI. He touched upon cloud parallelization, CPU-GPU parallelization, FPGA parallelization while introducing smart solvers.

In session 4, Mr. Rajkumar Nagpal, Synopsys, New Delhi cited a case study for system modeling for DDR3. He gave a brief on how the problem was diagnosed and how it was rectified by a valid packaging solution.

In session 5, Dr. C. Balaji, IIT Madras, Chennai presented his views on assessment of high heat flux thermal management techniques in electronics using solid liquid phase change material based heat sinks. He first gave as to why heat sinks are required. What are the constraints for

designing heat sinks and what is the need to have an optimal design. Then he gave the solution for optimizing heat sink design using multi objective optimization.

In the last session a panel discussion was held in which the participants put forward their queries to the experts which were answered. The workshop ended with distribution of certificates and vote of thanks by Pf. Rohit of IIT, Ropar.